28. (New) The device of Claim 27 wherein the depth of the halo implant is zero under the midpoint of the hard mask layer.

29. (New) The device of Claim 15 wherein the gate structure includes a layer of tungsten silicide between the hard mask layer and the substrate.

30. (New) The device of Claim 15 wherein the gate structure includes a layer of polycide between the hard mask layer and the substrate.--

REMARKS

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this application in view of the foregoing amendment and the following remarks. The Applicants originally filed Claims 1-20. Claims 15-19 were reintroduced in the present application. The Applicants presently amend Claim 15, add new Claims 21-30, and do not cancel any claims. Accordingly, Claims 15-19 and 21-30 are currently pending in the present application.

The Applicants also presently amend the Specification. However, these amendments merely correct typographical errors, and do not add any new subject matter.

I. Rejection of Claims 15 and 17-19 under 35 U.S.C. §102

The Examiner has rejected Claims 15 and 17-19 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,362,052 to Rangarajan, *et al.* ("Rangarajan"). However, Rangarajan fails to

anticipate independent Claim 15 and its dependent Claims 17-19 because Rangarajan fails to disclose each and every element of Claim 15. Specifically, Rangarajan fails to disclose a gate structure having a contoured upper layer of a hard mask material that varies in thickness across the gate structure. In contrast, Rangarajan merely discloses resist masks 34 on an ONO layer 24 at opposing sides of a bit line oxide region 50 (FIGs. 3-5; column 5, lines 40-53), that are not part of a gate structure and are only temporary elements (column 7, lines 27-31). Thus, the final structure taught in Rangarajan does not include the resist masks 34 or a contoured upper hard mask layer.

Accordingly, Rangarajan fails to disclose each and every element of independent Claim 15. Consequently, Rangarajan is not an anticipatory reference with respect to Claim 15 and its dependent claims 17-19. Therefore, the Applicants request the Examiner withdraw the §102 rejection with respect to Claims 15 and 17-19.

Rangarajan also fails to anticipate new Claims 21-30 because these claims are also dependent on Claim 15.

II. Rejection of Claim 16 under 35 U.S.C. §103

The Examiner has rejected Claim 16 under 35 U.S.C. §103 as being unpatentable over Rangarajan. However, as discussed above, Rangarajan fails to teach a gate structure having a contoured upper hard mask layer that varies in thickness across the gate structure, as recited in Claim 15. Moreover, in view of the mask regions 34 being employed only to form the bit line oxide region 50 and the halo implants thereabout, Rangarajan provides no suggestion to employ the mask regions 34 as a permanent portion of a gate structure in order to form halo implants under the gate structure. One skilled in the art would also find no motivation for such a modification in Rangarajan because

those skilled in the art understand that the construction and function of field oxide regions (*e.g.*, bit line oxide region 50) and halo implants thereabout are different than the construction and function of gate structures and halo implants thereunder.

The Examiner also concedes that Rangarajan fails to teach or suggest silicon dioxide being used as a hard mask layer and, therefore, provides an official notice asserting that silicon dioxide is a well known masking material which can also be used on top of a gate to protect against ion implantation damages. However, the combination of Rangarajan and the official notice fails to support a *prima facie* case of obviousness of Claims 15 and 16 because the Examiner has failed to provide support for combining such teachings and, instead, merely relies on hindsight to arrive at such a combination. Moreover, the Examiner has failed to provide support that one skilled in the pertinent art would combine the teachings of the official notice and Rangarajan in order to arrive at the presently claimed invention. Furthermore, the Examiner's official notice fails to cure the shortcomings of Rangarajan discussed above, because the official notice fails to teach, suggest or even mention a gate structure having a contoured upper hard mask layer that varies in thickness across the gate structure.

Accordingly, Rangarajan fails to teach or suggest a gate structure having a contoured upper hard mask layer that varies in thickness across the gate structure, as recited in Claim 15. Therefore, Rangarajan fails to teach or suggest each and every element of Claim 15 and its dependent claims. Accordingly, Rangarajan fails to support a *prima facie* case of obviousness of Claim 15 and its dependent claims. Consequently, the Applicants request the Examiner withdraw to withdraw the §103 rejection with respect to Claim 16, which is dependent on Claim 15.

Rangarajan also fails to support a *prima facie* case of obviousness of new Claims 21-30 because these claims are also dependent on Claim 15.

III. Additional References Made of Record

The Applicants believe that the additional references made of record and not relied upon by the Examiner are not particularly pertinent to the claimed invention, but the Applicants retain the right to address these references in detail, if necessary, in the future.

IV. Conclusion

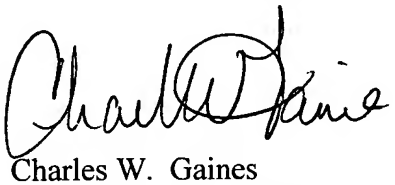
In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 15-19 and 21-30.

Attached hereto is a marked-up version of the changes made to the specification and the claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES & BOISBRUN, P.C.



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

(1) Please amend the paragraph at page 5, lines 17-23 as follows:

It should be readily appreciated that n-channel transistors may be similarly formed, but with an n-type source 24, an n-type channel [24] 30, an n-type drain 26, and lightly-doped p-type halo implants 42,44 (i.e., of a conductivity which is the opposite of the source and drain). CMOS devices may have both n-channel and p-channel in adjacent regions of a substrate.

(2) Please amend the paragraphs at page 7, lines 1-31 as follows:

A voltage adjust implant is performed while the n-well tub is defined. Dopant atoms, such as boron, are implanted into an upper region of the n-well 14 in the region at which the gate is to be formed to define a p-channel implant as shown in FIGURE 2. This implant is referred to as the threshold adjust implant and is used to set the threshold voltage at the gate. Preferably, the boron threshold adjust implant provides a nominal turn on (about 0.4 volts for 0.16 μm technology) for to-be-defined channel [24] 30 in both PMOS and NMOS devices.

The gate 22 layers are then deposited. Specifically, an oxide for the gate oxide layer 28 is grown over the substrate surface, for example, by thermal oxidation. Polysilicon for the gate 22 is then deposited over the gate oxide. Various techniques, such as physical deposition, chemical vapor

deposition, or epitaxial growth, may be used to perform this step. Preferably, an upper layer [34] 33 of tungsten silicide, is then deposited over the polysilicon, by, for example, sputtering.

A layer 60 of a hard mask material is then deposited on an upper surface of the gate -i.e., on an upper surface 62 of the tungsten silicide layer [34] 33. The mask material is one which is etched selectively over polysilicon or silicon. The hard mask material is preferably an oxide, such as silicon oxide, or silicon nitride. However, other oxides which are deposited by chemical vapor deposition (CVD) may also be used. The silicon oxide may be formed, for example, by LPCVD or PECVD using a plasma comprising tetraethylorthosilicate (TEOS), and optionally hydrogen, to a thickness of between about 500 and 2000Å, preferably, about 1000-1500Å.

(3) Please amend the paragraph at page 10, lines 16-32 as follows:

After the halo implant is created, dopant atoms are implanted into regions [36] 34 and 38 to form the heavily doped regions of the source and drain. The wafer W, which may have many such devices formed thereon is then annealed to repair the implant damage (restore the silicon lattice structure) and to activate the dopants (placing the dopant atoms on vacant sites). Finally, metal 20 and one or more intermediate layers 16 of an insulation material, such as a dielectric material of doped silicon dioxide are formed. The metal provides the necessary connections with other devices on the wager while the doped oxide serves as an intermediate dielectric to isolate the metal interconnect level from the polysilicon 32, 22. The steps for fabricating an actual MOS transistor involves many more steps. These steps are well known and are described in S.M. Sze, "VLSI Technology," 2nd. ed., New York: McGraw-Hill (1988).

IN THE CLAIMS:

(1) Please amend Claim 15 as follows:

15. (Amended) A MOS device comprising:

a gate structure on a semiconductor substrate, the gate structure having an upper layer of a hard mask material, the hard mask material being contoured such that it varies in thickness across the gate structure; and

a halo implant in the semiconductor substrate, the halo implant having a depth profile under the gate structure which follows at least a portion of the contour of the hard mask layer.

(2) Please add new Claims 21-30 as follows:

–21. (New) The device of Claim 15 wherein the hard mask layer is substantially dome-shaped.

22. (New) The device of Claim 15 wherein the hard mask layer contour has a top portion and side portions, wherein the depth profile of the halo implant under the gate structure follows the side portions of the hard mask layer contour.

23. (New) The device of Claim 22 further including a channel defined between regions of the halo implant, the regions defined by the depth profile following the side portions of the hard mask layer.

24. (New) The device of Claim 15 wherein the hard mask has a maximum thickness at a mid-point thereof and a minimum thickness at a periphery thereof.

25. (New) The device of Claim 24 wherein the minimum thickness is about zero.

26. (New) The device of claim 15 wherein a depth of the halo implant under an edge of the gate structure is substantially equal to a maximum thickness of the hard mask layer.

27. (New) The device of Claim 15 wherein the depth of the halo implant is substantially zero under a midpoint of the hard mask layer.

28. (New) The device of Claim 27 wherein the depth of the halo implant is zero under the midpoint of the hard mask layer.

29. (New) The device of Claim 15 wherein the gate structure includes a layer of tungsten silicide between the hard mask layer and the substrate.

30. (New) The device of Claim 15 wherein the gate structure includes a layer of polycide between the hard mask layer and the substrate.--